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FREESCALE SEMICONDUCTOR LAW DEPARTMENT

DATE: September 9, 2004

TO:	Office of Initial Patent Examination (ADDRESSEE)	(703) 308-1202 (EXTENSION)
	USPTO (LOCATION)	(703) 746-9195 (FAX UMBER)
FROM:	Pat Thomas for Joanna Chiu (SENDER)	(512) 996-6839 (EXTENSION)

TOTAL NUMBER OF PAGES 10 **(Including this page)**

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Docket No.: SC12888TH
Applicant: William C. Moyer et al.
Serial No.: 10/631,136
Art Unit: 2186
Filed: July 31, 2003

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	1 page Request for Correction of Filing Receipt
3.	x	1 page Copy of Filing Receipt Showing Changes Requested
4.	x	1 page Copy of Fee Transmittal Submitted with Application
5.	x	1 page Copy of Claims as Sumitted with Application

Paid by Deposit Account 503079, Freescale Semiconductor, Inc.: $0
If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE:

ON: 9-9-04 (Date) Pat Thomas (Signature)

FREESCALE SEMICONDUCTOR LAW DEPARTMENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William C. Moyer et al.	)	Examiner: Unassigned
Serial No.: 10/631,136	)	Group Art Unit: 2186
Filed: July 31, 2003	)	Docket No.: SC12888TH
For: PREFETCH CONTROL IN A DATA PROCESSING SYSTEM	)	

OFFICE OF INITIAL PATENT EXAMINATION
COMMISSIONER FOR PATENTS
ALEXENDRIA, VA 22313-1450

REQUEST FOR CORRECTION OF FILING RECEIPT

Applicants respectfully request correction of two errors on the USPTO Filing Receipt. In particular, through no fault of the Applicants, the number of total claims and the number of individual claims are incorrect. Applicants have provided a copy of the claims and the fee transmittal which were included with the original filing papers. Applicants respectfully request that total claims be changed to 23 and individual claims to 3.

A copy of the first page of the USPTO Filing Receipt showing the desired corrections is submitted with the present request.

Respectfully submitted,

9/8/04
Date

Joanna G. Chiu
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FEE TRANSMITTAL

Patent fees are subject to annual revision

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 844

	Complete	Known
Application Number		
Filing Date		
First Named Inventor		William C. Moyer
Examiner Name		
Group Art Unit		
Attorney Docket No.		SC12888TH

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 502117

Deposit Account Name: Motorola, Inc.

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)		Fee Paid
1001	750	2001	375	Utility filing fee	750
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 750

2. EXTRA CLAIM FEES

		Previously Paid**		Extra Claims		Fee from below		Fee Paid
Total Claims	23	20	=	3	X	18	=	54
Independent Claims	3	3	=	0	X	84	=	
Multiple Dependent						280	=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	* Reissue independent claims over original patent
1205	18	2205	9	* Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 54

**OR NUMBER PREVIOUSLY PAID, IF GREATER THAN STANDARD ALLOWANCE.

*For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late Provisional filing	
*1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for ex parte Reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1840*	1805	1840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1450	2254	725	Extension for reply within fourth month	
1255	1970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1300	2453	650	Petition to revive – unintentional	
1501	1300	2501	650	* Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of IDS	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	40
1809	750	2809	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

* Reduced by Basic Filing Fee paid SUBTOTAL (3) ($) 40

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Joanna G. Chiu	Registration No.	43,629	Telephone	(512)996-6839
Signature	Joanna G. Chiu	Date	7/31/03		

CLAIMS

1. A data processing system, comprising:

a first master;

storage circuitry, coupled to the first master, for use by the first master;

a first control storage circuit which stores a first prefetch limit;

a prefetch buffer; and

prefetch circuitry, coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry, said prefetch circuitry selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer, wherein the first prefetch limit controls how many prefetches occur between misses in the prefetch buffer.

2. The data processing system of claim 1, further comprising:

a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines from the storage circuitry into the prefetch buffer based on the first prefetch counter.

3. The data processing system of claim 1, further comprising:

a second master, wherein the storage circuitry is coupled to the second master and is for use by the second master; and

a second control storage circuit which corresponds to the second master and stores a second prefetch limit.

4. The data processing system of claim 3, wherein the first prefetch limit controls how many prefetches for the first master occur between misses in the prefetch buffer on read requests from the first master, and wherein the second prefetch limit controls how many prefetches for the second master occur between misses in the prefetch buffer on read requests from the second master.

5. The data processing system of claim 3, further comprising:

a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines for the first master from the storage circuitry into the prefetch buffer based on the first prefetch counter; and

a second prefetch counter, wherein the prefetch circuitry selectively prefetches a predetermined number of lines for the second master from the storage circuitry into the prefetch buffer based on the second prefetch counter.

6. The data processing system of claim 3, wherein the prefetch circuitry:

selectively prefetches the predetermined number of lines for the first master based on the first prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the first master; and

selectively prefetches the predetermined number of lines for the second master based on the second prefetch counter in response to at least one of a hit or a miss in the prefetch

buffer corresponding to an access request from the second master.

7. The data processing system of claim 1, wherein the prefetch circuitry selectively prefetches the predetermined number of lines in response to at least one of a hit or a miss in the prefetch buffer.

8. The data processing system of claim 1, wherein the first control storage circuit is programmable.

9. The data processing system of claim 1, further comprising a request monitor coupled to the first control storage circuitry, wherein the request monitor selectively updates the prefetch limit based on a number of buffer hits in the prefetch buffer accessed between two misses in the prefetch buffer.

10. A method for performing prefetch in a data processing system, comprising:

receiving a plurality of access requests from a master to access storage circuitry; and

using a prefetch limit to limit a number of prefetches performed between misses in a prefetch buffer resulting from at least a portion of the plurality of access requests.

11. The method of claim 10, further comprising providing a prefetch control circuit to store the prefetch limit.

12. The method of claim 10, wherein using the prefetch limit to limit the number of prefetches comprises:

counting prefetches after a miss in the prefetch buffer to determine when the prefetch limit is reached.

13. The method of claim 12, wherein each prefetch prefetches a single line from the storage circuitry.

14. The method of claim 13, wherein each single line prefetch is performed in response to at least one of a hit or a miss in the prefetch buffer.

15. A method for performing prefetch in a data processing system, comprising:

receiving a read request from a master to access storage circuitry;

determining whether the read request results in a hit or a miss in a prefetch buffer;

if the read request results in a hit, selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value; and

if the read request results in a miss, performing a demand fetch in response to the read request and setting the prefetch counter to a second value.

16. The method of claim 15, wherein selectively performing the prefetch of the predetermined number of lines is further based on

whether or not the predetermined number of lines is already present in the prefetch buffer.

17. The method of claim 16, further comprising:

prefetching the predetermined number of lines from the storage circuitry and updating the prefetch counter when the read request results in a hit, the prefetch counter has not reached the first value, and the predetermined number of lines is not already present in the prefetch buffer.

18. The method of claim 17, wherein the second value corresponds to a prefetch limit and wherein updating the counter comprises decrementing the prefetch counter.

19. The method of claim 17, wherein the first value corresponds to a prefetch limit and wherein updating the counter comprises incrementing the prefetch counter.

20. The method of claim 16, further comprising:

not prefetching from the storage circuitry when the read request results in a hit and the prefetch counter has reached the first value.

21. The method of claim 15, further comprising prefetching a predetermined number of lines from the storage circuitry when the read request results in a miss.

22. The method of claim 15, wherein selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value is performed such that the predetermined number of lines comprises only a single line.

23. The method of claim 15, further comprising:

receiving a master identifier corresponding to the master; and

selecting the prefetch counter from a plurality of prefetch counters based on the master identifier.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/631,136	07/31/2003	2186	750	SC12888TH	4	~~18~~ 23	~~2~~ 3

CONFIRMATION NO. 3949

23125
MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
7700 WEST PARMER LANE MD: TX32/PL02
AUSTIN, TX 78729

FILING RECEIPT

"OC000000011859397"

Date Mailed: 02/10/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

William C. Moyer, Dripping Springs, TX;
Lea Hwang Lee, Austin, TX;
Afzal M. Malik, Austin, TX;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 10/28/2003

Projected Publication Date: 02/03/2005

Non-Publication Request: No

Early Publication Request: No

Title

Prefetch control in a data processing system